



TET ESTEL AS
ESTONIA

April
2017

Series
TL233-500

Avalanche Press-Pack Thyristor Type TL233-500

Center amplifying gate

Guaranteed avalanche power dissipation in reverse direction

Designed for traction and industrial applications

Maximum mean on-state current	I_{TAV}	500 A				
Maximum repetitive peak off-state and reverse voltage	U_{DRM} U_{RRM}	600 ÷ 1100 V				
Turn-off time	t_q	80; 100; 125 μs				
U_{DRM}, U_{RRM}, V	600	700	800	900	1000	1100
Voltage code	6	7	8	9	10	11
$T_{vj}, ^\circ C$	- 60 ÷ 140					

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	TL233-500	Conditions
I_{TAV}	Mean on-state current	A	500 850	$T_c=102^\circ C$, $T_c=55^\circ C$ 180° half-sine wave, 50 Hz
I_{TRMS}	RMS on-state current	A	785	$T_c=102^\circ C$
I_{TSM}	Surge on-state current	kA	9,0 10,0	$T_{vj}=140^\circ C$ $T_{vj}=25^\circ C$ tp=10 ms $U_R=0$
I^2t	Limiting load integral	kA^2s	405 500	$T_{vj}=140^\circ C$ $T_{vj}=25^\circ C$
U_{DRM}, U_{RRM}	Repetitive peak off-state and reverse voltage	V	600÷1100	$T_j \min \leq T_{vj} \leq T_{jM}$ 180° half-sine wave, 50 Hz Gate open
U_{DSM}, U_{RSM}	Non-repetitive peak off-state and reverse voltage	V	660÷1210	$T_j \min \leq T_{vj} \leq T_{jM}$ 180° half-sine wave tp=10 ms, Single pulse Gate open
(diT/dt) crit	Critical rate of rise of on-state current : non - repetitive repetitive	A/ μ s	250 125	$T_{vj}=140^\circ C$; $U_D=0,67 U_{DRM}$, Gate pulse : 10V,5 Ω , 1 μ s rise time, 10 μ s
U_{RGM}	Peak reverse gate voltage	V	5	$T_j \min \leq T_{vj} \leq T_{jM}$
P_{RSM}	Surge reverse power dissipation	kW	40	$T_{vj}=140^\circ C$; tp = 10 μ s 180° half-sine wave
T_{stg}	Storage temperature	$^\circ C$	-60÷80	
T_{vj}	Junction temperature	$^\circ C$	-60÷140	

CHARACTERISTICS

U_{TM}	Peak on-state voltage	V	1,9	$T_{vj}=25^\circ C$, $I_{TM}=3,14 I_{TAV}$
$U_{T(TO)}$	Threshold voltage	V	0,9	$T_{vj}=140^\circ C$
R_T	On-state slope resistance	m Ω	0,63	1,57 $I_{TAV} < I_T < 4,71 I_{TAV}$
I_{DRM} I_{RRM}	Repetitive peak off-state and reverse current	mA	35 35	$T_{vj}=140^\circ C$, $U_D = U_{DRM}$ $U_R = U_{RRM}$

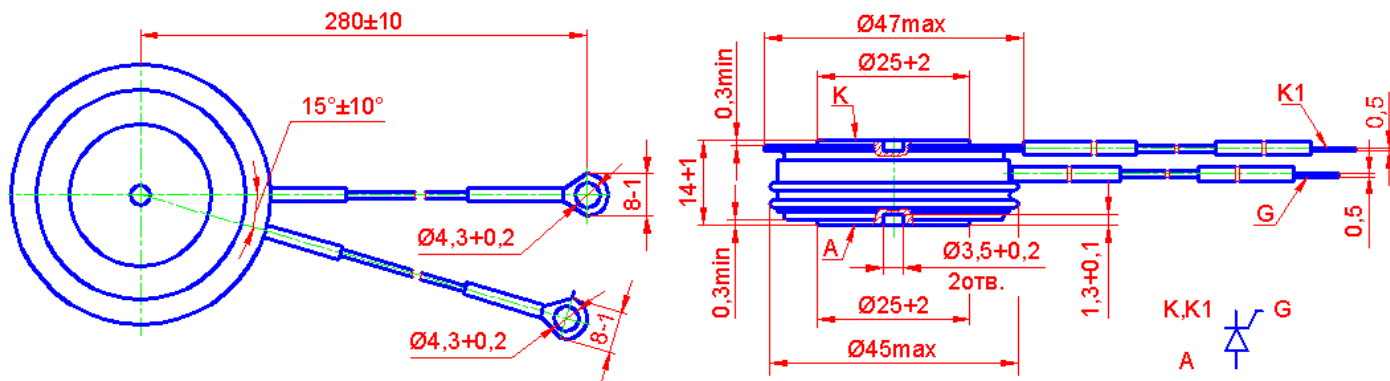
CHARACTERISTICS

Symbols and parameters		Units	TL233-500	Conditions
I_L	Latching current	A	0,7	$T_{vj}=25^{\circ}\text{C}, U_D=12\text{V}$ Gate pulse : 10V, 5 Ω , 1 μs rise time, 10 μs
I_H	Holding current	A	0,3	$T_{vj}=25^{\circ}\text{C}, U_D=12\text{V}$, Gate open
U_{GT}	Gate trigger direct voltage	V	2,5 5,0	$T_{vj}=25^{\circ}\text{C}$, $T_{vj}=-60^{\circ}\text{C}$ $U_D=12\text{V}$
I_{GT}	Gate trigger direct current	A	0,3 0,85	$T_{vj}=25^{\circ}\text{C}$, $T_{vj}=-60^{\circ}\text{C}$
U_{GD}	Gate non-trigger direct voltage	V	0,4	$T_{vj}=140^{\circ}\text{C}$, $U_D = 0,67 U_{DRM}$
I_{GD}	Gate non-trigger direct current	mA	6	Direct gate current
tgd	Delay time	μs	1,6	$T_{vj}=25^{\circ}\text{C}, U_D=500\text{V}$ $I_{TM} = 500 \text{ A}$
tgt	Turn-on time	μs	3,2	Gate pulse : 10V, 5 Ω , 1 μs rise time, 10 μs
tq	Turn-off time	μs	80÷125	$T_{vj}=140^{\circ}\text{C}$, $I_{TM}=500 \text{ A}$ $di_R/dt = 10 \text{ A}/\mu\text{s}$, $U_R=100\text{V}$ $U_D = 0,67 U_{DRM}$ $du_D/dt=50 \text{ V}/\mu\text{s}$
Qrr	Recovered charge	μC	780	$T_{vj}=140^{\circ}\text{C}$, $I_{TM}=500 \text{ A}$ $di_R/dt=10 \text{ A}/\mu\text{s}$, $U_R=100\text{V}$
trr	Reverse recovery time	μs	6	
Irrm	Peak reverse recovery current	A	260	
(du_D/dt)crit	Critical rate of rise of off-state voltage	V/ μs	500 1000	$T_{vj}=140^{\circ}\text{C}$, $U_D = 0,67 U_{DRM}$ Gate open
Rthjc	Thermal resistance junction to case	$^{\circ}\text{C}/\text{W}$	0,045	Direct current, double side cooled

ORDERING

	TL	233	500	11	7	4	
	1	2	3	4	5	6	

1. Avalanche thyristor
2. Design version
3. Mean on-state current, A.
4. Voltage code (11=1100 V)
5. Critical rate of rise of off-state voltage ($6 \geq 500 \text{ V}/\mu\text{s}$, $7 \geq 1000 \text{ V}/\mu\text{s}$)
6. Group of turn-off time ($du_D/dt=50 \text{ V}/\mu\text{s}$, $X2 \leq 125 \mu\text{s}$, $4 \leq 100 \mu\text{s}$, $B3 \leq 80 \mu\text{s}$, 0-not limited)



Tightening torque : 9 ÷ 12 kN

Weight : 120 grams